스위치 개방 고장을 고려한 3-레벨 NPC 인버터의 동적 등가 모델

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Dynamic Equivalent Model of Three-Level NPC Inverters with Consideration of Open-Switch Faults

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ABSTRACT

This article proposes a model of a 3-level neutral-point-clamped (NPC) inverter capable of representing the inverter during both normal operation and single open-switch faults. Conventional inverter modeling methods provide accurate voltages and currents during normal operation but fail to do so during open switch faults. To address this limitation, a novel model is proposed that takes into account the effect of capacitor voltages, alternative conduction paths, and current directions. The proposed model can be implemented as a digital twin of a 3-level NPC inverter as it represents faulty states accurately. The accuracy of the proposed model is compared with waveforms obtained from the experiment. The proposed model has errors of 0.133 A, 0.138 A, and 0.158 A in three-phase load currents.

1. Introduction

Three-phase three-level inverters are being widely implemented in the field of renewables and motor drives. Modeling of the three-phase three-level inverter is generally approached in four ways; switching state function-based model, observer-based model, mixed logical dynamic model, and adaptive model [1]-[3]. For a thorough investigation of the operation of the inverter, faulty operations of the inverter should be investigated, not only the normal operation. In general, switch modeling of an inverter takes into account only the normal operation of the inverters, while the obtained equations are not capable of representing the faulty operation of the inverter. So, such a model cannot be used for fault analysis or the representation of an inverter in a real-time simulation system. Recent works have addressed this research gap. One approach developed a generalized phase arm model for NPC three-level inverter [4]. However, this approach fails to consider the effect of other phase switches on the pole voltage of the faulty phase arm. As such, the developed model would not accurately represent the system in faulty conditions [2]. In this paper, a model for a three-level NPC inverter is presented that includes the effect of other phase switches, current direction, and voltage imbalance on two DC-link capacitors during an open switch fault.

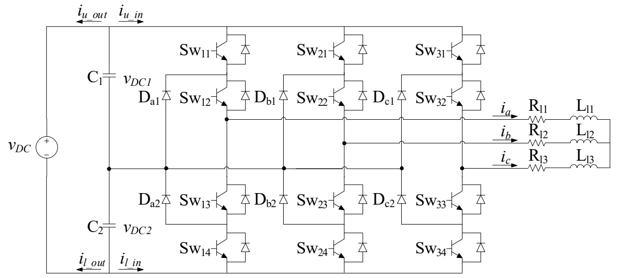

Fig. 1: Three-level NPC inverter.

2. Proposed Dynamic Modeling of 3-Level NPC Inverters

Fig. 1 shows the topology of a 3-level NPC inverter. Here, Sw_{mn} represents the switching states of all the involved switches, where m ranges from 1 to 3 for three-phase arms and n ranges from 1 to 4. V_{DC} is the DC voltage source connected to the two capacitors C_1 and C_2 with voltages V_{DC1} and V_{DC2} respectively. Unbalanced capacitor voltage can be modeled using different variables for voltages of upper and lower capacitors. I_a, I_b, and I_c are 3-phase load currents and V_{ab}, V_{bc}, and V_{ca} are the line-to-line voltages.

For an RL load, the line-to-line voltage V_{ab} is also dependent on the direction of load currents. So, a functions sg_{Ia} is defined as,

$$\left\{ sg_{Ia} = \begin{cases} 1, I_a \geq 0 \\ 0, I_a < 0 \end{cases} \right. . \tag{1}$$

Accounting for the current direction, variables y_{i1}, y_{i2}, y_{j1}, and y_{j2} are defined as,

$$\begin{aligned} y_{i1} = &(\overline{(Sw_{11}+Sw_{13})\times(Sw_{12}+Sw_{14})})\times sg_{Iau}\times((Sw_{22}\times Sw_{32}\times Sw_{21}+Sw_{22}\times Sw_{32}\times Sw_{31})\times(V_{DC1}\times\overline{sg_{nu}}+V_{DC2}\times sg_{nu}) \\ &+(Sw_{21}+Sw_{31})\times sg_{nu}\times(V_{DC1}-V_{DC2})-(Sw_{24}+Sw_{34})\times Sw_{14}\times(V_{DC1}-V_{DC2})+Sw_{22}\times Sw_{23}\times Sw_{32}\times Sw_{33}\times Sw_{14}\times V_{DC1}) \end{aligned} . \tag{2}$$

$$\begin{aligned} y_{i2} = &(\overline{(Sw_{21}+Sw_{23})\times(Sw_{22}+Sw_{24})})\times sg_{Ibu}\times((Sw_{32}\times Sw_{12}\times Sw_{31}+Sw_{32}\times Sw_{12}\times Sw_{11})\times(V_{DC1}\times\overline{sg_{nu}}+V_{DC2}\times sg_{nu}) \\ &+(Sw_{31}+Sw_{11})\times sg_{nu}\times(V_{DC1}-V_{DC2})-(Sw_{34}+Sw_{14})\times Sw_{24}\times(V_{DC1}-V_{DC2})+Sw_{32}\times Sw_{33}\times Sw_{12}\times Sw_{13}\times Sw_{24}\times V_{DC1}) \end{aligned} . \tag{3}$$

$$\begin{aligned} y_{j1} = &(\overline{(Sw_{11}+Sw_{13})\times(Sw_{12}+Sw_{14})})\times\overline{sg_{Ial}}\times((Sw_{22}\times Sw_{32}\times Sw_{21}+Sw_{22}\times Sw_{32}\times Sw_{31})\times(V_{DC1}\times\overline{sg_{nu}}+V_{DC2}\times sg_{nu}) \\ &+(Sw_{21}+Sw_{31})\times sg_{nu}\times(V_{DC1}-V_{DC2})-(Sw_{24}+Sw_{34})\times Sw_{14}\times(V_{DC1}-V_{DC2})+Sw_{22}\times Sw_{23}\times Sw_{32}\times Sw_{33}\times Sw_{14}\times V_{DC1}) \end{aligned} . \tag{4}$$

$$\begin{aligned} y_{j2} = &(\overline{(Sw_{21}+Sw_{23})\times(Sw_{22}+Sw_{24})})\times\overline{sg_{Ibl}}\times((Sw_{32}\times Sw_{12}\times Sw_{31}+Sw_{32}\times Sw_{12}\times Sw_{11})\times(V_{DC1}\times\overline{sg_{nu}}+V_{DC2}\times sg_{nu}) \\ &+(Sw_{31}+Sw_{11})\times sg_{nu}\times(V_{DC1}-V_{DC2})-(Sw_{34}+Sw_{14})\times Sw_{24}\times(V_{DC1}-V_{DC2})+Sw_{32}\times Sw_{33}\times Sw_{12}\times Sw_{13}\times Sw_{24}\times V_{DC1}) \end{aligned} . \tag{5}$$

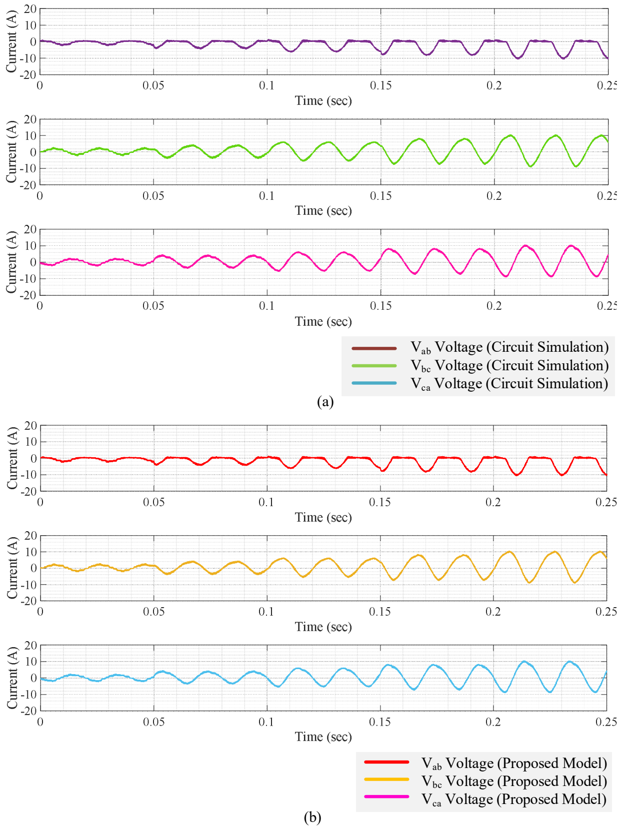

Fig. 2: Load current waveforms for different modulation indices and Sw11 open switch fault based on (a) Circuit simulation. (b) Proposed model.

Finally, the line-to-line voltages, V_{abu} and V_{abl} are obtained. V_{abu} is the line-to-line voltage when the open-circuit fault is in the upper two switches, while V_{abl} is the line-to-line voltage when the open circuit is in the lower two switches.

$$V_{abu}=y_1-\frac{y_{i1}-y_{i2}}{2}, \quad (6)$$

$$V_{abl}=y_1+\frac{y_{j1}-y_{j2}}{2}. \quad (7)$$

3. Simulation and Experimental Results

To check for the accuracy of the proposed model, a comparison between the proposed model and the circuit block simulation is made in Fig. 2. Fig. 2 compares the load currents for the system during the open switch fault of Sw_{11} at different modulation indexes. A balanced three-phase load of 10 Ω resistance and 3 mH inductance is connected to the inverter.

The parameters for the experiment are listed in Table 1. DSP TMS320F28335 is used as a controller for the NPC inverter. DC input voltage is taken as 175 V while the other parameters remain the same as listed in Table 1. At the start, the NPC inverters are normally operated and individual faults are manually imposed upon the hardware after some time. Three open switch faults are performed and the outputs obtained from the experiment are compared against the output obtained from the proposed model as shown in Fig. 3. The absolute average median errors are calculated to be 0.113 A, 0.134 A, and 0.158 A for 3-phase load currents.

Table 1. Parameters for simulation and experiment.

Parameters	Symbol	Values
DC input voltage	V_{DC}	200 V
Load resistance	R_{11}, R_{12}, R_{13}	10 Ω
Load inductance	L_{11}, L_{12}, L_{13}	3 mH
DC-link capacitor	C_1, C_2	4700 μF
Inverter frequency	f	50 Hz
Switching frequency	f_{sw}	5 kHz

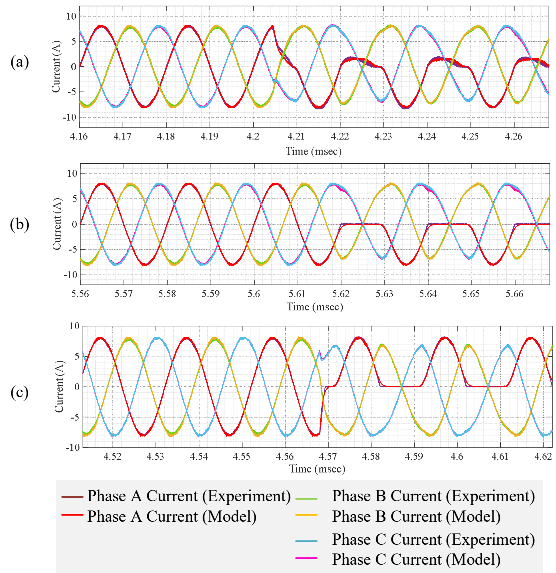

Fig. 3: Load current of proposed model and hardware for open switch fault of (a) Sw_{11}. (b) Sw_{12}. (c) Sw_{13}.

4. Conclusions

A switch-based modeling approach for three-phase three-level NPC inverters, incorporating considerations such as alternate conduction paths, individual capacitors, and current direction during faulted conditions has been presented in this article. With the ability to predict system behavior in both normal and faulty scenarios, the proposed model can be used to develop a reliable digital twin. The median absolute errors of the proposed model have been calculated to be 0.133 A, 0.138 A, and 0.158 A for three-phase load currents through the experiment.

References

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